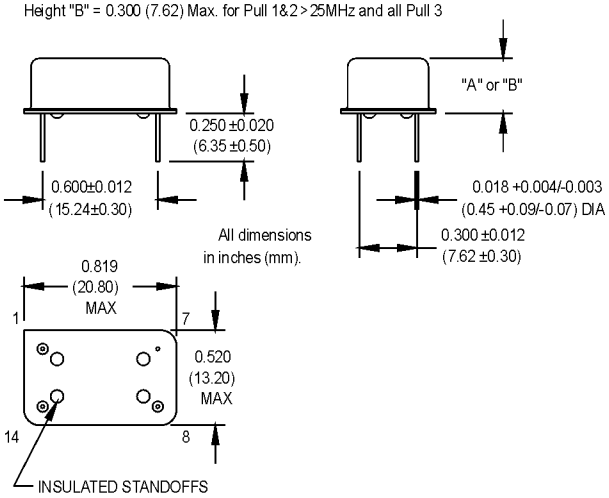
查询MV18V3AD供应商

MV Series

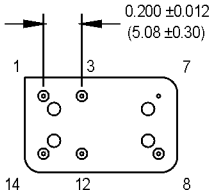
14 DIP, 5.0 Volt, HCMOS/TTL, VCXO

- General purpose VCXO for Phase Lock Loops (PLLs), Clock Recovery, Reference Signal Tracking, and Synthesizers
- Frequencies up to 160 MHz
- Tri-state Option Available

Height "A" = 0.200 (5.08) Max. for Pull 1&2 < 25 MHz
Height "B" = 0.300 (7.62) Max. for Pull 1&2 > 25MHz and all Pull 3



OPTIONAL 6-PIN PACKAGE
WITH TRISTATE



Pin Connections

PIN	FUNCTION
1	Control Voltage
3	Tristate (6-Pin Pkg. Only)
7	Ground
8	Output
12	N/C (6-Pin Pkg. Only)
14	+Vdd

Ordering Information

MV 1 3 V 2 C D -R 00.0000 MHz

Product Series
Temperature Range
1: 0°C to +70°C **2:** -40°C to +85°C
6: -20°C to +70°C
Stability
1: ±1000 ppm **2:** ±500 ppm **3:** ±100 ppm
4: ±50 ppm **5:** ±35 ppm **6:** ±25 ppm
***8:** ±20 ppm
Output Type
V: Voltage Controlled **T:** Tristate
Pull Range (Vc = .5 to 4.5V)
1: ±50 ppm min. **2:** ±100 ppm min.
3: ±200 ppm min. ("B" package only)
Symmetry/Logic Compatibility
A: 40/60 CMOS/TTL **C:** 45/55 HCMOS
Package/Lead Configurations
D: DIP; Nickel Header **G:** Gull Wing; Nickel Header
RoHS Compliance
Blank: non-RoHS compliant part
-R: RoHS compliant part
Frequency (customer specified)

*Contact factory for availability

Electrical Specifications

PARAMETER	Symbol	Min.	Typ.	Max.	Units	Condition/Notes
Frequency Range	F	1.5		160	MHz	See Note 1
Operating Temperature	T_A	(See Ordering Information)				
Storage Temperature	T_S	-55		125	°C	
Frequency Stability	ΔF/F	(See Ordering Information)				
Aging 1st Year Thereafter (per year)		 0.6 0.5		 0.6 0.5	 ppm ppm	 < 52 MHz / ≥ 52 MHz < 52 MHz / ≥ 52 MHz
Pullability/APR		(See Ordering Information)				Over control voltage
Control Voltage	Vc	0.5	2.5	4.5	V	
Linearity				10	%	Positive Monotonic Slope
Modulation Bandwidth	fm	10			kHz	
Input Impedance	Zin	50k			Ohms	
Input Voltage	Vdd	4.75	5	5.25	V	
Input Current	Idd		25 35 55	40 60 90	mA mA mA	1.5 to 24.999 MHz 25 to 69.999 MHz 70 to 160 MHz
Output Type						HCMOS/TTL
Load		10 TTL or 50 pF 5 TTL or 15 pF				See Note 2 1.5 to 54.999 MHz 55 to 160 MHz
Symmetry (Duty Cycle)		(See Ordering Information)				See Note 3
Logic "1" Level	Voh	90% Vdd Vdd -0.5			V V	HCMOS load TTL load
Logic "0" Level	Vol			10% Vdd 0.5	V V	HCMOS load TTL load
Rise/Fall Time 1.5 to 54.999 MHz 55 to 160 MHz	Tr/Tf			 6 / 10 1.5 / 5	 ns ns	See Note 4 TTL/HCMOS TTL/HCMOS
Tri-state Function		Input Logic "1" or floating: output active Input Logic "0": output disables to high-Z				
Start up Time			5		ms	
Phase Jitter @ 38.88 MHz @ 155.52 MHz	ϕJ		 0.3 10	 1 15	 ps RMS ps RMS	 Integrated 12 kHz - 20 MHz Integrated 12 kHz - 20 MHz
Phase Noise (Typical) @ 38.88 MHz @ 155.52 MHz	**10 Hz** -71 -62	**100 Hz** -104 -93	**1 kHz** -134 -113	**10 kHz** -151 -115	**100 kHz** -153 -114	**Offset from carrier**

1. Frequencies above 90 MHz utilize a PPL design. Fundamental and PLL designs are available for other frequencies. Contact factory.
2. TTL load – see load circuit diagram #1. HCMOS load – see load circuit diagram #2
3. Symmetry is measured at 1.4 V with TTL load, and at 50% with HCMOS load.
4. Rise/Fall times are measured between 0.5 V and 2.4 V for TTL load, and between 10% Vdd and 90% Vdd for HCMOS load.

MtronPTI reserves the right to make changes to the product(s) and service(s) described herein without notice. No liability is assumed as a result of their use or application.